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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/002,726 | 10/24/2001 | Kenneth Y. Ogami | CYPR-CD01171M | 2851 |

7590 08/28/2006

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| EXAMINER |
|---|
| SIEK, VUTHE |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/002,726 | OGAMI ET AL. | |
| | Examiner | Art Unit | |
| | Vuthe Siek | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8 and 10-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-17 and 19-37* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/002,726 and communications filed on 06/14/06. Claims 1-8 and 10-37 remain pending in the application, where claim 9 is canceled and claims 38-41 have been canceled as to non-elected claims.

2. Note that indication of allowable independent claims 1 and 30 and their dependency has been withdrawn due to ambiguous claim language as described in below.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 11, 22 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitations of "a description of hardware resources" (claims 1 & 30), "a text based description" (claims 11 & 22), "configuration information" (claims 1, 11, 22 & 30), "a selected configuration" (claims 1, 11, 22 & 30) and "interrupt vector" (claim 30) are indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In light of the specification as whole, the claimed limitations lack antecedent basis. The claimed limitations must be clear and precise as to what each of the claimed limitations is refereed to in light of the specification. Failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention would cause a claim construction problem because one can interpret the claimed limitations in many ways.

There each of the claimed limitations as described above should be clearly defined. Note that all dependent claims on the based claims that are not described are also virtually rejected based on the rejected based claims.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 11, 13-17 and 19-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Insenser Farre et al. (6,460,172).

7. As to claims 11 and 22, Insenser Farre et al. teach a microprocessor based mixed signal field programmable integrated device and prototyping methodology for configure and dynamically reconfigure all the programmable features of the system with the microprocessor, between countless other possibilities (see abstract, summary; col. 3 lines 15-48). As a result, a set of cells rather than the whole chip as shown in Fig. 1 can be configured and reconfigured dynamically to produce a countless user-programmable integrated circuit (col. 5 lines 3-19). The Fig. 1 describes the claimed features of microcontroller (microprocessor for controlling), dynamically configurable blocks including digital blocks and analog blocks, a set of library macros and cells for accessing and selection of configurable blocks including their descriptions (Fig. 1, col. 3

lines 15-67 describe overall system; col. 4 lines 15-67 describe digital blocks and analog blocks; col. 5 lines 1-34 describe microprocessor; col. 3 line 62 to col. 4 line 15, describe that a countless system can be produced). A microprocessor accessed configuration contexts for configure and dynamically reconfigure the programmable features to produce a user-programmable integrated circuit that include a microcontroller (col. 4 lines 1-65). Thus, Insenser Farre et al. teach accessing a description of hardware resources/a text based description of dynamically configurable blocks. The system as shown in Fig. 1 comprises a processor, memories, configurable blocks including digital blocks, analog blocks that are selectable from a set of library macros and cells to configure and dynamically reconfigure whole or partial system (Fig. 1 and its description; col. 3 lines 15-67; col. 4 lines 1-65).

8. As to claims 13-17 and 23-29, Insenser Farre et al. teach configuration contexts of programmable features and description of programmable features for use in configure and dynamically refigure the IC as shown in Fig. 1 (col. 4 lines 1-65) (these descriptions as text based description and non-executable software). Insenser Farre et al. also teach a set of library macros and cells, user-programmable integrated circuit, and user circuit and the microprocessor configure and dynamically reconfigure the programmable blocks to produce a countless system as desired according to applications (at least see col. 1 lines 62-67, col. 2 lines 1-14, col. 2 lines 27-67). Note that the microprocessor generates microprocessor instructions (commands) during configure and dynamically reconfigure the programmable blocks, where all main parts of microprocessor, digital blocks, analog blocks and memories are interfaces and

embedded on a single chip name Field Programmable System-on-a-Chip (FIPSOC) (col. 2 lines 1-67). The system as taught by Insenser Farre et al. comprises integrated tools (embedded software) (col. 2 lines 23-40). The set of library macros and cells comprises macros and cells have name for use during configure and dynamically reconfigure whole or partial system (at leas see col. 2 lines 1-67, Fig. 1 and its description).

9. As to claims 19-21, Insenser Farre et al. teach FIPSOC as described in Fig. 1, where integrated tools are used to assist the embedded microprocessor to configure and dynamically reconfigure whole or partial system to produce a countless system as desired according to applications needed (col. 2 lines 22-40; col. 5 lines 3-67; col. 6 lines 1-6). The countless system produced by FIPSOC as taught by Insenser Farre et al. enable the use to new hardware configuration by selecting from the set library macros and cells as described in the patent.

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al. (6,460,172) in view of Zizzo (6,578,174).

12. As to claim 12, Insenser Farre et al. does not explicitly teach the description of dynamically configurable blocks is substantially compliant with extensible markup

language (XML). Zizzo teaches a method and system for chip design using remotely located resources comprising circuit design platform to facilitate the design of an IC by making it easier for designers to locate and incorporate available virtual component blocks into new designs include using a universal data interface format or mark-up language (XML) is preferably used as a primary data interface between the various components of the system and the details XML are well-known to those in the art of computer programming (col. 7, 9). Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to implement the description of hardware resources with extensible markup language (XML) because its universal data format, the XML language would be easy to implement and preferably used as primary data interface between various components (EDAs) of the design platform.

***Remarks***

13. Applicants argued that Insenser Farre et al. does not teach accessing a text based description of a plurality of dynamically configurable blocks. Examiner disagrees. Insenser Farre et al. teach using a microprocessor to configure and reconfigure programmable features within the FIPSOC architecture that includes a microcontroller (see summary). The microprocessor accessed configuration contexts of programmable features for configure and dynamically reconfigure the programmable features to produce a user programmable integrated circuit (col. 4 lines 1-65). Note that the configuration contexts describe programmable features including a microcontroller for configure and dynamically reconfigure the programmable features of the integrated circuit design to produce a countless user programmable integrated circuit. A library

macros is provided for storing configurable programmable macros or programmable features including microcontroller (col. 3 lines 14-65). When the microprocessor accessed configuration contexts for configuring and reconfiguring programmable features that include microcontroller the microprocessor generated configuration information for use to produce a user programmable integrated circuit. Examiner disagrees with applicants whom assert that Insenser Farre does not teach a text based description. The configuration contexts for example are text based description. The description of programmable features in column 4 is a text based description. Since the claimed limitations are ambiguous as described in above 112/2 rejection. The description as taught by Insenser Farre met the claim limitation. The library macros stored programmable macros for selection as recited in the claims. Thus, Insenser Farre teach the selecting step. As described in above rejection, Farre does not teach the description of dynamically configurable blocks is compliant with extensible markup language (XML). Examiner relied on Zizzo that teach the claimed limitation. Because XML is easy to use, to take advantage of the XML language, it would have been obvious to one skilled in the art to describe the dynamically configurable blocks as taught by Insenser Farre in XML format. Since the claimed language is ambiguous as described in above 112/2 rejection; the library macros as taught by Insenser Farre met the claimed limitation of selecting step. It appears that the claims do not clearly recite that a microcontroller is dynamically reconfigured using the XML language. If so, Examiner is requested applicants to show how a microcontroller is dynamically reconfigure using the XML language.

***Allowable Subject Matter***

14. Claims 1-8, 9 and 30-37 are allowed over the prior art of record if rewritten to include all limitations of based claims and if rewritten to overcome the rejection under 112/2. The prior art of record does not teach or fairly suggest generating an interrupt vector table for use by embedded software, wherein a plurality of interrupts included in said interrupt vector table are generated by said selected configuration along with all claim limitations as recited in the claims.

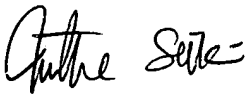
15. Claim 18 is allowed over the prior art of record if rewritten to include all limitations of based claims and if rewritten to overcome the rejection under 112/2. The prior art of record does not teach or fairly suggest generating an interrupt vector table for use by embedded software, wherein a plurality of interrupts included in said interrupt vector table are generated by said selected configuration

***Conclusion***

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



VUTHE SIEK
PRIMARY EXAMINER